

REMARKS

Claims 1-25 remain pending in the current Application. Claim 14 has been amended to address an informality. No other amendments to the claims have been made herein. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claim Rejections under 35 U.S.C. § 112

Claim 14 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, claim 14 was rejected for lack of antecedent basis for the limitation "the address" because multiple addresses were mentioned in the base claim. Applicants have amended claim 14 to point out that "the address" is one of the addresses mentioned in the base claim and that "the address" corresponds to the sequence signals mentioned in claim 14. Applicants respectfully submits that sufficient antecedent basis has been provided for the limitation "the address," and respectfully requests that the Examiner withdraw the rejection of claim 14 in light of Applicants' amended claim 14.

Claim Rejections under 35 U.S.C. § 102

Claims 1-9, 13-17, and 21-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,604,877 to Hoyt et al. (hereinafter "Hoyt"). Claims 10-12 and 18-20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,205,536 to Toyohiko Yoshida (hereinafter "Yoshida"). Applicants respectfully traverse the rejections.

MPEP § 2131 provides that in order to anticipate a claim, the reference must teach every element of the claim. Specifically, MPEP § 2131 states (emphasis added):

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"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "When a claim covers several structures or compositions, either generically or as alternatives, the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) (claim to a system for setting a computer clock to an offset time to address the Year 2000 (Y2K) problem, applicable to records with year date data in "at least one of two-digit, three-digit, or four-digit" representations, was held anticipated by a system that offsets year dates in only two-digit formats). See also MPEP § 2131.02. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Note that, in some circumstances, it is permissible to use multiple references in a 35 U.S.C. 102 rejection. See MPEP § 2131.01.

Applicants respectfully assert that the cited references simply fail to teach each and every element as set forth in Applicants' claims.

Claims 1, 3, 13 and 24 and their Dependent Claims

Claims 1, 3, and 24 each claim a processing system for accessing memory that includes the following limitations:

- an address bus ... ;
- a data bus for receiving information from memory; and
- first means for generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address, a second sequence signal that when negated indicates that the current address is not sequential to the previous address, and a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the current address, if it is an instruction address, is sequential to the immediately preceding instruction address.

Claims 3 and 24 claim that the generation of the sequence signals is performed by a fetch unit. In addition, claim 3 and claim 24 each add the limitations of a decode control unit and an execution unit for generating branch conditions and data addresses. However, the key differences between Hoyt and Applicants' claimed invention lie in Applicants' claimed sequence signals and the fact that Hoyt does not teach or suggest any of such control signals.

Claim 13 claims a processing system for accessing memory that includes the following limitations:

- an execution unit;
- a decode control unit;
- a fetch unit, coupled to the execution unit and the decode unit, for providing addresses on an address bus which may be sequential, and providing a first sequence signal and a second sequence signal for each address provided on the address bus wherein the first sequence signal indicates whether each address provided on the address bus may be sequential to an immediately preceding address on the bus and a second sequence signal that indicates whether each address provided on the bus is sequential to the immediately preceding address on the bus.

Claim 13 claims the first and second sequence signals whereas claims 1, 3, and 24 each claim three sequence signals. As explained herein, however, Hoyt does not teach or suggest any of Applicants' claimed signals. Consequently, the Office Action fails in its burden under 35 U.S.C. § 102 as Hoyt does not teach each and every limitation as found in Applicants' claims.

The Office Action contends that Hoyt teaches Applicants' claimed invention. As discussed below, Applicants respectfully disagree and assert that Hoyt simply does not teach Applicants' claimed invention. First, Applicants' claimed invention claims three separate signals: a first sequence signal, a second sequence signal, and a third sequence signal. Characteristics of each signal is also set forth in the claim for each of the respective signals. Applicants' claimed signals are used to communicate with different types of memory. As shown throughout Applicants' figures and specification describing these signals, these signals are sent at different times in order to allow for longer or shorter setup times for different types of memory. These signals, SEQ* 124, ASEQ* 122, and ISEQ* 112, may also have other uses in other applications. The Office Action asserts that Hoyt teaches each of these "signals." Upon closer inspection of the Hoyt reference, however, it is clear that Hoyt does not teach or suggest any of these signals.

The Office Action asserts that Hoyt teaches:

"generating a first sequence signal that when negated indicates that the current address may not be sequential to the previous address," citing col. 8, lines 41-58. However, at col. 8, lines 41-58, Hoyt teaches:

Before each instruction fetch, the Instruction Fetch Unit 30 passes a current Instruction Pointer (IP) to the Branch Target Buffer Circuit 40 to learn if there is an upcoming branch instruction that directs the microprocessor to a nonsequential address. The Branch Target Buffer Circuit 40 examines the Branch Target Buffer Cache 41 using the Instruction Pointer, looking for an upcoming branch instruction. If the Branch Target Buffer Circuit 40 finds an upcoming branch instruction, a Branch Target Buffer Cache 41 "hit" has occurred and the Branch Target Buffer Circuit 40 makes a branch prediction using the branch information from the Branch Target Buffer Cache 41. A detailed description of the Branch Target Buffer Circuit 40 can be found in the copending patent titled "Method and Apparatus for predicting Branches in a CISC processor", Ser. No. 08/177,155, filed Jan. 4, 1994 and is hereby incorporated by reference.

As can be seen in the cited section of Hoyt, the reference is not "generating a first sequence signal..." as claimed by Applicants. Instead, Hoyt is teaching a way of resolving a Return From Subroutine instruction using the Branch Target Buffer (BTB) to determine if there is an upcoming branch instruction in the BTB. Hoyt further uses this information to make a branch prediction. Importantly, however, Hoyt never teaches or suggests *generating a signal* using this information. In order to reject Applicants' claim under § 102, the reference must teach each and every limitation (see MPEP § 2131). Here, Hoyt derives information from a BTB to determine if a "hit" has occurred. Also, Hoyt is comparing the current address to a subsequent address when making the determination. In sharp contrast, Applicants claim comparing the current address with a previous address to generate the signal.

Likewise, the Office Action asserts that Hoyt teaches Applicants' limitation of "generating a second sequence signal that when negated indicates that the current address is not sequential to the previous address," citing Table 2 and column 9, lines 59-62 of Hoyt. Again, the Office Action's reliance on Hoyt for such teaching is misplaced. Table 2 outlines various branch types that can be encountered along with the branch target buffer logic that is performed. The section of Hoyt at column 9, lines 59-62 follows the table and states, "If the branch outcome decision is taken, then the Branch Target Buffer Circuit 40 predicts a branch to the address

provided within the branch target address field of the Branch Target Buffer Cache 41 entry.” Once again, Hoyt does not teach or suggest generating any signals as claimed by Applicants. Instead, Hoyt is describing a well-known method of using branch history to predict whether a branch should be taken. In the cited section, Hoyt merely describes prediction of a branch to an address within the branch target address field of the BTB’s cache. Again, this section of Hoyt suffers from the same shortcomings as the previous section. Namely, this section of Hoyt does not teach or suggest generating any signals when the branch outcome decision is made and, secondly, Hoyt is concerned with the current address and a subsequent address (the branch target address), while Applicants’ claimed limitation is directed to the current address and the previous address not being sequential to one another.

The differences between Applicants’ claimed invention and Hoyt are even more compelling with respect to the third sequence signal. Applicants’ claimed limitation is for “a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to an immediately preceding instruction address and when asserted indicates that the current address, if it is an instruction address, is sequential to the immediately preceding instruction address.” The Office Action asserts that Hoyt teaches this limitation, citing column 2, lines 3-9 of Hoyt. Applicants’ second signal is negated when the current address is not sequential to the previous address and Applicants’ third signal is negated when the current address is an instruction address and is not sequential to an immediately preceding instruction address. In other words, Applicants’ claimed invention handles both data and instruction addresses. The second signal is negated when the current address is not sequential to the previous address irregardless of the type of address (data or instruction address), while Applicants’ third signal is only used when the current address is an instruction address. On the other hand, Hoyt only uses instruction addresses as its branch prediction logic would not work using data addresses. The cited section of Hoyt is as follows:

However, if the branch prediction mechanism mispredicted the branch instruction, the microprocessor is executing instructions down the wrong path and therefore accomplishes nothing. When the microprocessor eventually detects the mispredicted branch, the microprocessor must flush the instructions that were speculatively fetched from the instruction pipeline and restart execution at the correct address. (col. 2, lines 3-9).

In the cited section, Hoyt is describing the situation of a mispredicted branch. This well-known aspect of branch prediction appears in the "background" section of Hoyt and simply describes that, when a branch has been mispredicted, the instructions that have been fetched from the instruction pipeline must be flushed. This has nothing to do whatsoever with Applicants' claimed limitation. The Office Action includes a rather lengthy discussion trying to explain how a branch misprediction is the same as Applicants' "generating a third sequence signal..." However, when analyzed, the discussion contained in the Office Action further emphasizes the differences between Applicants' claimed invention and the teachings of Hoyt.

The Office Action states that Hoyt teaches:

generating a third sequence signal that when negated indicates that the current address, if it is an instruction address, is not sequential to the previous address that was an instruction address. See column 2, lines 3-9, and note that the third signal would be the branch outcome signal, which determines if a misprediction has occurred or not. That is, if the branch was predicted taken, for instance, when the third signal is negated (signifying correct prediction), then the current address, which is an instruction address, is not sequential. On the other hand, if the third signal is asserted (signifying incorrect prediction), then the branch was really not supposed to be taken, and the current address is sequential to the previous address. Note that the examiner is defining the previous address as the branch instruction address, and the current address is the address from which to fetch after the previous address.

Not only does Hoyt not teach or suggest generating a "signal" when the current address is not sequential to the previous address, but by the time a misprediction occurs the address with the branch that was mistakenly taken has long been processed. That is the essence of a misprediction – when, as Hoyt describes, the misprediction is discovered, the microprocessor is currently executing sequential instructions down the wrong path. In response, the microprocessor must flush the instructions from the pipeline and restart execution at the correct address. The Examiner tries to redefine the previous address as the branch instruction address and the current address as the address from which to fetch after the previous address (the "branch to" address). However, this re-definition simply won't work. Applicants' claim that the signal is negated when the current (instruction) address is not sequential to "an immediately preceding instruction address ..." In other words, Applicants' preceding instruction address is immediately before the current instruction address.

The Examiner states that the "third signal would be the branch outcome signal, which determines if a misprediction has occurred or not." The Examiner then wants to define the current address as the "branch to" address and the previous address as the branch instruction address. However, using the Examiner's own definitions and assumptions, the "branch outcome signal" (not really taught by Hoyt) is generated when the misprediction occurs. When the misprediction occurs, the "current" and "previous" addresses defined by the Examiner have long since been processed, thereby necessitating that the pipeline be flushed (as discussed by Hoyt). If, on the other hand, the misprediction occurred when the "branch to" instruction was the "current address," as defined by the Examiner, mispredictions would never take place because the microprocessor would immediately take the other path. In the microprocessor arts using instruction pipelines, this feat would mark a utopian event. However, this feat suggested by the Examiner is simply not possible nor does Hoyt teach or even suggest this possibility.

Claims 2, 4 - 9, 21 and 23 each depend, directly or indirectly, on claims 1 and 3 and therefore are allowable for at least the same reasons that claims 1 and 3 are allowable, as set forth above.

Applicants' claim 13, as mentioned above, includes the first two signals but does not include the third signal that was claimed in claims 1, 3, and 24. As explained above, Hoyt does not teach or suggest generating any of the signals taught and claimed by Applicants. In claim 13, Applicants claim that the "first sequence signal indicates whether each address provided on the address bus may be sequential to an immediately preceding address on the bus..." In rejecting Applicants' claim 13, the Office Action states that, in Hoyt, "the first signal would be the BTB hit signal, as a hit denotes that a branch has been encountered and that the current address may be sequential to the previous address depending on the predicted direction of the branch" (citing col. 8, lines 42-53 of Hoyt). Applicants respectfully submit that the Office Action is misapplying the teachings of Hoyt. In Hoyt, if a hit is encountered in the BTB, the address is not sequential to the previous address because the BTB is a table of branch addresses and, by definition, the "branch to" address will not be sequential to the current address. Moreover, Hoyt never teaches or suggests "generating a signal" in response to analyzing the BTB. In attempting to show that Hoyt teaches Applicants' claimed "second sequence signal," the Office Action states:

In addition, a second signal inherently is produced which indicates whether the program counter is to be incremented or whether it is to be replace (sic) by a

predicted address. This second signal would be a signal that indicates whether the PC should be incremented (in the case there's no branch) or if the PC is to be replaced (in case there is a branch, the PC needs to be replaced with the predicted branch address). When the second signal is in the first state, where the PC is to be incremented, since a branch does not occur, the address is sequential to the previous address.

Applicants respectfully disagree with the Examiner and submit that Hoyt does not teach a second signal that is "inherently" generated. Instead, as the Office Action points out, a program counter is either incremented or is loaded with a branch address. Nowhere does Hoyt teach or suggest "generating a signal" with this information. When the program counter is loaded with either an incremented address or a "branch to" address it is simply updated with no signal lines used to send a signal that the program counter is either sequential or is not sequential to a previously loaded address. Hoyt simply does not teach or suggest sending or generating a signal indicating whether the address in the program counter is sequential to the previous address that was in the program counter.

Claims 14 – 17, 22, and 25 each depend either directly or indirectly on claim 13 and, therefore, are allowable for at least the same reasons that claim 13 is allowable.

Claims 10 and 18 and their Dependent Claims

Claims 10-12 and 18-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by Yoshida (U.S. Patent No. 6,205,536). Applicants respectfully traverse the rejections.

As pointed out above, a claim is only anticipated if the prior art teaches each and every limitation claimed by Applicants.

Claim 10 claims a processing system for fetching instructions and data, including the limitations of:

- an address bus for providing a current address for retrieving a first instruction, a previous address for retrieving a second instruction, and a data address for retrieving data, wherein the data address occurs before the current address and after the previous address, and wherein the current address follows the previous address without any intervening addresses for retrieving instructions;
- a data bus for retrieving the first and second instructions and the data; and

- a fetch unit, coupled to the address bus and the data bus, for generating a first sequence signal that when asserted for the current address indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address.

Claim 18 claims a processing unit that includes the limitations of:

- an execution unit;
- a decode control unit;
- a fetch unit, coupled to the execution unit and the decode unit, for providing instruction and data addresses on an address bus and providing a first sequence signal that indicates whether each instruction address provided on the address bus is sequential to an immediately preceding instruction address even if a data address is provided between the instruction address and the immediately preceding instruction address.

Each of claims 10 and 18 include the limitation of a "sequence signal" that indicates whether a sequential relationship exists between addresses. The Office Action contends that Yoshida teaches generating a sequence signal. Upon closer inspection of Yoshida, however, it is clear that Yoshida never teaches or suggests generating or using a sequence signal.

The Office Action states that Yoshida teaches:

a fetch unit, coupled to the address bus and the data bus, for generating a first sequence signal that when asserted for the current address indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address. Note that from column 10, lines 30-36, that Yoshida has taught branch prediction for branch instructions, which would be a type of instruction represented in Fig. 27. Even though Yoshida is silent as to how the branch prediction (first signal) is performed, it is inherent that when predicting branches, they may be taken or not taken. Clearly, if a branch is predicted not taken, then the current address is sequential to the previous address. That is, the system begins fetching from the address immediately following the address of the branch instruction. On the other hand, if the branch is predicted taken, then the current address may not be sequential to the previous address. That is, the system begins fetching from the target address of the branch instruction. However, since the prediction won't be validated or invalidated until the branch is finally executed, the fetching from the

target is merely speculative, as opposed to known. (Office Action, page 16, emphasis added)

The fact that the Office Action admits that Yoshida is silent as to how the branch prediction (first signal) is performed is a telltale sign that Yoshida does not teach or suggest providing a signal that indicates whether addresses are sequential to one another. A review of the portions of Yoshida cited in the Office Action buttresses this assertion.

Figure 27 of Yoshida shows various signals used for data access, common, and instruction access. While over ten separate signals are shown in Figure 27, not one of the signals is used as a sequential indicator. Yoshida's description of Figure 27 is as follows:

FIG. 27 shows a data read cycle with zero wait (C1), an instruction read cycle with zero wait (C2), a data read cycle with zero wait (C3), an instruction read cycle with one wait state (C4), a data write cycle with zero wait (C5), a data read cycle with one wait state (C6), an instruction read cycle with zero wait (C7), a data write cycle with zero with (C8), an instruction read cycle with zero wait (C9) and an instruction read cycle with zero wait (C10), as well as the initial portion of the next data read cycle.

A data access cycle and an instruction access cycle can be overlapped by two clock cycles of CLK, as, for example, in the case of (C1) and (C2) or the case of (C8) and (C9). However, two data access cycles or two instruction access cycles cannot be executed in an overlapped fashion, for example, in the case of (C5) and (C6) or (C9) and (C10).

A succeeding data access cycle is started when the preceding data access cycle is complete. Specifically, a data address is output by CPU 10 onto address bus A(0:31) 14 synchronically with a rise in BCLK when BAT(0:2) is 000: DDC# is then asserted, thus completing the bus cycle.

In a data access cycle, the data address strobe DAS# is asserted with a delay of a half cycle of the CLK clock relative to the address output. Also, the data strobe DS# is asserted with a delay of one and a half cycles of CLK.

A read cycle and a write cycle are distinguished from each other by the read/write R/W# signal.

In a data write cycle, data is output to data bus 17 with a delay of one and a half cycles of CLK relative to the address output.

In a data read cycle, when the DDC# signal is asserted, the value on data bus 17 at the falling edge of CLK is read by CPU 10.

Where the preceding instruction access cycle is complete, the instruction access cycle starts when the address from the data access cycle is no longer output. Specifically, the instruction address is output to address bus 14 synchronically with a rising edge of BCLK when BAT(0:2) is 001. IDC# is then asserted, thus completing the bus cycle.

In an instruction access cycle, the instruction address strobe IAS# is asserted with a delay of a half cycle of CLK with respect to the output of an instruction address. The instruction strobe IS# is asserted one and a half cycles of CLK after the address output. Then, when the IDC# is asserted, the value on the instruction bus 16 at the falling edge of CLK is read by CPU 10. Where a data access cycle and an instruction access cycle are needed at the same time, the data access cycle, which has priority, is started first.

In the data access cycle and the instruction access cycle, the access time is extended by an integer number of clock cycles of BCLK until DDC# and IDC# are respectively asserted.

In CPU 10, where HREQ# has been asserted, after both the data access cycle and the instruction access cycle being executed at that time have completed, the HACK# signal is asserted and CPU 10 gives the right of bus master to another device. When HREQ# is deasserted, HACK# is deasserted and CPU 10 takes back the right of bus master.

Note that nowhere does Yoshida teach or suggest that any of the numerous signals shown in Figure 27 is used to transmit sequence information. Yet, despite this serious shortcoming, the Office Action persists in asserting that Yoshida teaches Applicants' claimed limitation of claims 10 and 18. The Office Action further cites col. 10, lines 30-36 as teaching Applicants' sequence signal. However, upon review of the cited section, it is abundantly clear that Yoshida is bereft of any such teaching:

There is also a second stage decoder which further decodes an output of the FHW decoder and the NFHW decoder and calculates an entry address to the micro ROM, a branch predicting mechanism for performing branch prediction of a conditional branch instruction, and an address calculation conflict checking mechanism for checking pipeline conflicts in calculating an operand address.

In the cited section, the output of a "first half word" decoder and the "not first half word decoder" is decoded to calculate an entry address to a branch predicting mechanism and an address calculation conflict mechanism. Nowhere in the cited section does Yoshida teach or suggest a sequence signal that indicates whether two addresses are sequential to one another. The Office Action ties the section recited above to Figure 27. However, as explained above, neither cited section teaches or suggests generating or providing a sequence signal as claimed by Applicants. Furthermore, Applicants performed an electronic search of Yoshida and revealed that Yoshida never even mentions "sequential instructions," "sequential address," "sequential signal" or any other "sequential" or "sequence" term that could be remotely used in support of the Office Action. Consequently, Yoshida fails as a 102 reference in that it does not teach each

and every limitation claimed by Applicants. Therefore claims 10 and 18 are allowable over Yoshida. Claims 11, 12, 19 and 20 each depend, either directly or indirectly on claims 10 and 18 and, therefore, are allowable for at least the same reasons that claims 10 and 18 are allowable.

Conclusion

Applicants submit that the remaining claims in the Application are in condition for allowance and a Notice of Allowance is respectfully requested. If a discussion with Applicants' representative would be helpful in addressing any issues of patentability, Applicants respectfully request that the Examiner contact Applicants' attorney using the contact information provided below.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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